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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/028,276	02/24/1998	SHIGERU ATSUMI	1701.73982	4461

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EXAMINER	
ECKERT II, GEORGE C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	09/028,276	ATSUMI, SHIGERU	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *10-12 and 15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,21-26,28-30 and 32-41* is/are rejected.

7)☒ Claim(s) *14,27,31 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated November 23, 2004 in which claims 1, 21 and 32 were amended, has been entered. Claims 1-42 are pending with claims 10-12 and 15-20 withdrawn.

Drawings

2. The drawings were received on January 25, 2005. These drawings are acceptable.

Specification

3. The objection to the disclosure based on informalities is withdrawn based on applicant's amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 21-26, 28 and 32-39 rejected under 35 U.S.C. 103(a) as being unpatentable over 5,188,976 to Kume et al. in view of JP 3-196677 to Soeda. Regarding claims 1, 21 and 32, Kume teaches in figures 15-18 a semiconductor integrated circuit device comprising:

a semiconductor substrate 11 on which a plurality of transistors having gate insulation films of three or more different thicknesses are formed. In figures 15 and 16, Kume teaches

transistors are formed in the Memory Transistor Area having an insulation layer 16 formed to a thickness of 10nm (col. 12, lines 45-47), that transistors are formed in the First Peripheral Circuit MOS Area having an insulation layer 38 formed to a thickness of 35nm (col. 13, lines 9-11) and that transistors are formed in the Second Peripheral Circuit MOS Area having an insulation layer 39 formed to a thickness of 18nm (col. 13, lines 7-9).

Kume does not teach an input/output terminal formed on the substrate, wherein a transistor physically connected directly to the input/output terminal is a transistor other than a transistor having the thinnest gate insulation film. Soeda teaches, in figure 1, an input/output terminal 8 formed on a semiconductor substrate (see Means for Solving Problems which indicates the pad is on a substrate), wherein a transistor 12' or 13' physically connected directly to the input/output terminal is a transistor other than a transistor having the thinnest gate insulation film (e.g 12'/13' have thick gate oxide while transistors 14 and 15 of the internal circuit 11 have thinner gate oxide). Kume and Soeda are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Kume using the thick oxide transistors of Soeda. The motivation for doing so, as is taught by Soeda, is that by forming the transistor that is connected to the input/output terminal to have a thicker gate oxide provides electrostatic withstand voltage protection without deteriorating response characteristics of the internal circuit (*Constitution*). Therefore, it would have been obvious to combine Kume and Soeda to obtain the invention of claims 1-8, 21-26, 28 and 32-39.

Regarding claims 2 and 3, Soeda also teaches in figure 1 a power supply terminal V to which an external power supply voltage is applied and a ground terminal G, wherein a transistor

5' connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film (e.g. 14 and 15) and the transistor 5' has a current path connected between the power supply and ground. Regarding claims 4-7, Soeda teaches that the device also includes an interface circuit 10 comprising transistor 12' which is a transistor other than a transistor with the thinnest gate insulation film, that transistor 12' is connected directly to a power supply terminal and has a current path connected between the power supply and a ground terminal, and is part of an input buffer circuit. Regarding claims 4-6 and 8, Soeda also teach an embodiment in figure 2 where transistor 22, which has a thick gate oxide, is connected directly to an input/output terminal 21, is connected between a power supply terminal V and ground G, and is in an interface circuit 19 which is considered an output buffer (see the translation, page 4, third full paragraph).

Regarding claim 21, Soeda teaches in figure 2 an input/output terminal 21 formed on the semiconductor substrate, wherein a transistor (e.g. 22) connected directly to the terminal 21, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film. Regarding claims 22-26 and 28, Soeda teach in figure 2 that the device further comprises a power supply terminal V, a ground terminal G, such that transistor 22 is connected directly to the power supply terminal and has a current path to ground, that transistor 22 is part of an interface circuit 19, and that the interface circuit is an output buffer circuit.

Regarding claims 32-39, as discussed above, Soeda teaches that the transistor connected directly to the input/output terminal and having a thick gate oxide is always so connected.

5. Claims 9, 13, 29, 30, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume in view of Soeda as discussed above and further in view of applicant's admitted prior art as shown in figure 3. Kume and Soeda made obvious the device of claims 4, 24 and 35 as discussed above, including that the interface circuit included transistors having thicker gate oxide than transistors of the internal and protected circuits, but did not expressly teach the device wherein the interface circuit comprised a level shifter and output buffer or that the device comprised a regulator circuit providing a signal to the level shifter. Applicant's admitted prior art teaches in figure 3, an interface having an output buffer circuit 102, a level shifter 103 and a regulator circuit 101 which provides a signal to the level shifter, the level shifter converting the signal to a power supply voltage for supply to an external terminal.

Kume, Soeda and applicant's prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Kume and Soeda further comprising the interface as instantly claimed. The motivation for doing so, as is taught by applicant's admitted prior art, is that such a regulator circuit will lower a voltage level to prevent damage to logic or other internal circuitry while the level shifter will increase the output of the internal circuitry to produce a viable output. Therefore, it would have been obvious to combine Kume, Soeda and Applicant's prior art to obtain the invention of claims 9, 13, 29, 30, 40 and 41.

Allowable Subject Matter

6. Claims 14, 27, 31 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to all claims have been considered but are moot in view of the new grounds of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER